IN THE SPECIFICATION:

Please amend paragraph **[0001]** as follows:

[0001] This application is a divisional of application Serial No. 10/150,901, filed May 17, 2002, ~~pending,~~ now U.S. Patent 7,348,215, issued March 25, 2008, which is related to U.S. Patent Application Serial No. 09/944,465 filed August 30, 2001, now U.S. Patent ~~No.~~ 6,756,251, issued June 29, 2004, and entitled METHOD OF MANUFACTURING MICROELECTRONIC DEVICES, INCLUDING METHODS OF UNDERFILLING MICROELECTRONIC COMPONENTS THROUGH AN UNDERFILL APERTURE, and to the following U.S. Patent Applications also filed May 17, 2002: Serial No. 10/150,893, now U.S. Patent ~~No.~~ 7,145,225, issued December 5, 2006, entitled INTERPOSER CONFIGURED TO REDUCE THE PROFILES OF SEMICONDUCTOR DEVICE ASSEMBLIES AND PACKAGES INCLUDING THE SAME AND METHODS; Serial No. 10/150,892, entitled METHOD AND APPARATUS FOR FLIP-CHIP PACKAGING PROVIDING TESTING CAPABILITY; Serial No. 10/150,516, now U.S. Patent ~~No.~~ 7,112,520, issued September 26, 2006, entitled SEMICONDUCTOR DIE PACKAGES WITH RECESSED INTERCONNECTING STRUCTURES AND METHODS FOR ASSEMBLING THE SAME; Serial No. 10/150,653, now U.S. Patent ~~No.~~ 7,161,237, issued January 9, 2007, entitled FLIP CHIP PACKAGING USING RECESSED INTERPOSER TERMINALS; and Serial No. 10/150,902, now U.S. Patent ~~No.~~ 6,975,035, issued December 13, 2005, entitled METHOD AND APPARATUS FOR DIELECTRIC FILLING OF FLIP CHIP ON INTERPOSER ASSEMBLY.

Please amend paragraph **[0007]** as follows:

[0007] Recent trends in packaging are moving with increasing rapidity toward flip chip attachment due to improved electrical performance and greater packaging density. However, flip chip attachment is not without problems, such as the high cost for a third metal reroute of bond pads from the middle or periphery of a die to a two-dimensional array which, in turn, may result in overlong and unequal-length electrical paths. In addition, many conventional flip chip techniques exhibit a lack of consistent reliability of the interconnections between the chip and the

interposer or other carrier substrate as a result of the increased ~~miniaturization~~ miniaturization, as well as difficulties in mutual alignment of the die and carrier substrate to effect such interconnections. Effective rerouting of bond pads may also be limited by die size.

Please amend paragraph **[0008]** as follows:

[0008] Further, flip chip packages for a bumped semiconductor die employing an interposer may be undesirably thick due to the combined height of the die and interposer. This is due to the use in conventional packaging techniques of relatively costly interposers comprising dual conductive layers having a dielectric member sandwiched therebetween, the bumped semiconductor die resting on and connected to traces of the conductive layer on one side of the interposer and electrically connected to traces of the conductive layer on the opposing side, conductive vias extending therebetween. Finally, underfilling a flip chip-attached semiconductor die to a carrier substrate with dielectric filler material can be a lengthy and often unreliable process, and the presence of the underfill makes reworking of defective assemblies ~~difficult~~ difficult, if not impossible.

Please amend paragraph **[0009]** as follows:

[0009] Other difficulties with conventional packages include an inability to accommodate die size reductions, or "shrinks," as a given design progresses through several generations without developing new interposer designs and tooling. As more functionality is included in dice, necessitating a greater number of inputs and outputs (I/Os), decreased spacing or pitch between the I/Os places severe limitations on the use of conventional interposers. In addition, with conventional packages, a die is not tested until package assembly is complete, resulting in excess cost since a defective die or die and interposer assembly is not detected until the package is finished. For example, United States Patent 5,710,071 to Beddingfield et al. discloses a fairly typical flip chip attachment of a semiconductor die to a substrate and a method of underfilling a gap between the semiconductor die and substrate. In particular, the semiconductor die is attached ~~facedown~~ face down to the substrate, wherein conductive bumps on the die are directly bonded to bond pads on the upper surface of the substrate, which provides

the gap between the die and substrate. The underfill material flows through the gap between the semiconductor die and the substrate via capillary action toward an aperture in the substrate, thereby expelling air in the gap through the aperture in the substrate in an effort to minimize voids in the underfill material. However, such an underfilling method still is unnecessarily time consuming due to having to underfill the entire semiconductor die. Further, the flip chip attachment technique disclosed in United States Patent 5,710,071 exhibits difficulties in aligning the conductive bumps with the bond pads on the substrate and requires the expense of having a third metal reroute in the substrate.

Please amend paragraph **[0011]** as follows:

[0011] The present invention relates to methods and apparatus for assembling and packaging individual and multiple semiconductor dice with a carrier substrate in a flip chip-type arrangement. The present invention provides a flip ~~chip~~ chip-type semiconductor device assembly substantially reduced in height or depth in comparison to conventional interposer-based flip ~~chip~~ chip-type semiconductor device assemblies and with improved mechanical and electrical reliability of the interconnections between a semiconductor die and a carrier substrate in the form of an interposer, while also improving ease of alignment for attaching the semiconductor die to the carrier substrate and eliminating the requirement for a third metal ~~reroute~~ reroute, as well as reducing the time for optional dielectric underfilling of the flip ~~chip~~ chip-type semiconductor device assembly.

Please amend paragraph **[0012]** as follows:

[0012] The flip ~~chip~~ chip-type semiconductor device assembly of the present invention includes a conductively bumped semiconductor die assembled active surface, or ~~face, down~~ face down with an interposer substrate. The present invention includes multiple recesses formed from one surface of the interposer substrate and through the dielectric layer thereof to conductive elements in the form of conductive terminals or traces on the opposing surface, the recesses configured in a predetermined recess pattern that corresponds substantially with the bond pad, and hence conductive bump, pattern or configuration of the bumped semiconductor die. Such

predetermined recess patterns may include, for example, a single or double row center bond pad configuration, an I-shaped bond pad configuration and a peripheral bond pad configuration.

Please amend paragraph **[0013]** as follows:

[0013] An adhesive element may be optionally disposed between the semiconductor die and interposer substrate to mutually secure same, in addition to any bond between the conductive bumps and terminals or traces. The adhesive element may comprise a tape having a thickness, which may be used to provide and control a vertical standoff between the active surface and the interposer substrate and to increase compliancy of the attachment of the semiconductor die and interposer ~~substrate~~ substrate, as well as facilitating rework. In addition, the adhesive element assists to resolve minor variances in vertical travel of die pick-and-place equipment used to place a semiconductor die on the interposer substrate and helps maintain the die securely in position on the interposer substrate during subsequent handling, fabrication steps and transportation from one location to another.

Please amend paragraph **[0014]** as follows:

[0014] The flip ~~chip~~ chip-type semiconductor device assembly is assembled so that the conductive bumps on the semiconductor die are disposed in the recesses formed in the interposer substrate, the recesses being sized and configured to receive the bumps on the bumped semiconductor die so that they are submerged within the recesses to an extent that the active surface of the semiconductor die may sit directly against the surface of the interposer substrate onto which the recesses open. Thus, there is a reduction in the height of the flip ~~chip~~ chip-type semiconductor device assembly relative to conventional interposer-based flip ~~chip~~ chip-type semiconductor device assemblies due to the disposition of the conductive bumps within the recesses, which allows for the conductive bumps on the semiconductor die to be of larger size for increased reliability without increasing the overall height or depth of the flip ~~chip~~ chip-type semiconductor device assembly while avoiding the need for a third metal reroute on the semiconductor die. Even if an adhesive element using a tape is employed, the conductive bumps

may still be substantially completely received within the recesses, but for the small vertical standoff provided by the tape.

Please amend paragraph **[0016]** as follows:

[0016] The semiconductor device assembly of the present invention may also be configured with one or more openings extending through the interposer substrate at a location or locations from the surface facing away from the semiconductor die to provide communication between the one or more openings to each of the multiple recesses in the interposer substrate. This configuration facilitates dispensing of dielectric filler material through the opening or openings into the recesses and around the bumps. The opening or openings may be substantially coincident with the configuration of recesses and comprise gaps between conductive ~~pad~~ pads or terminal portions of conductive traces extending across the recesses or may comprise slots over or laterally offset from the recesses and in communication therewith and, if offset, a side of each recess being open to the slot. In the first and second instances, dielectric filler material may be introduced directly into the recesses through the gaps between the sides of the conductive trace extending over each recess and the periphery of the recess wall adjacent the trace. In the latter instance, dielectric filler material may be introduced into the slots to travel laterally therefrom into the recesses. Further, if a vertical standoff is employed between the interposer substrate and the semiconductor die, dielectric filler material may be introduced through a slot or other opening through the interposer substrate in the center region thereof and caused to flow therefrom into the recesses through the mouths thereof, even if not in communication with the opening, and to the periphery of the semiconductor die (if desired) through the standoff. This aspect of the present invention substantially enhances underfill integrity while decreasing process time.

Please amend paragraph **[0017]** as follows:

[0017] The flip ~~chip~~ chip-type semiconductor device assembly of the present invention may also include solder balls or other discrete external conductive elements attached to the conductive traces extending from the terminals over the surface of the interposer substrate facing away from the flip chip-type semiconductor die. The discrete external conductive elements are

employed to interconnect the semiconductor device assembly with higher-level packaging such as a carrier substrate, for example, in the form of a printed circuit board. The semiconductor die of the flip ~~chip~~ chip-type semiconductor device assembly may be fully or partially encapsulated by a dielectric encapsulation material or may be left exposed.

Please amend paragraph **[0018]** as follows:

[0018] In another aspect of the present invention, a heat transfer element may be included with the flip ~~chip~~ chip-type semiconductor device assembly. In particular, the heat transfer element may be included on the surface of the interposer substrate facing the semiconductor die, the active surface of the semiconductor die, or the back side of the semiconductor die. Such heat transfer element may be used to lower the operating temperature of the ~~assembly~~ assembly, as well as to prevent thermal fatigue.

Please amend paragraph **[0019]** as follows:

[0019] The flip ~~chip~~ chip-type semiconductor device assembly of the invention may include an unencapsulated semiconductor die, a partially encapsulated semiconductor die, or a fully encapsulated semiconductor die.

Please amend paragraph **[0020]** as follows:

[0020] The interposer substrate of the present invention may also be assembled with a plurality of semiconductor dice at a wafer or partial wafer level, wherein a wafer or partial wafer including a plurality of unsingulated semiconductor dice is attached ~~facedown~~ face down to a like-sized interposer substrate with bumps on the wafer or partial wafer submerged in recesses formed in the interposer substrate. Filler material may be dispensed through openings in the interposer substrate, after which the wafer or partial wafer and interposer substrate may be diced into individual flip ~~chip~~ chip-type semiconductor device assemblies. Encapsulation may be performed at least partially at the wafer level and completed, if desired, after being diced into individual semiconductor assemblies.

Please amend paragraph **[0022]** as follows:

[0022] In another aspect of the present invention, the flip ~~chip~~ chip-type semiconductor device assembly is mounted to a circuit board in a computer or a computer system. In the computer system, the circuit board is electrically connected to a processor device which electrically communicates with an input device and an output device.

Please amend paragraph **[0028]** as follows:

[0028] FIG. 3 is a simplified cross-sectional side view ~~take~~ taken along line 3-3 in FIG. 1;

Please amend paragraph **[0031]** as follows:

[0031] FIGS. ~~6A - 6B~~ 6A and 6B illustrate a first method of mounting a semiconductor die ~~facedown~~ face down to an interposer substrate in a flip chip-type semiconductor device assembly according to the present invention;

Please amend paragraph **[0032]** as follows:

[0032] FIGS. ~~7A - 7B~~ 7A and 7B illustrate a second method of mounting a semiconductor die ~~facedown~~ face down to an interposer substrate in a flip ~~chip~~ chip-type semiconductor device assembly according to the present invention;

Please amend paragraph **[0033]** as follows:

[0033] FIGS. 8A - 8D illustrate a third method of mounting a semiconductor die ~~facedown~~ face down to an interposer substrate in a flip ~~chip~~ chip-type semiconductor device assembly according to the present invention;

Please amend paragraph **[0034]** as follows:

[0034] FIGS. ~~9A - 9B~~ 9A and 9B illustrate a variant of the third method of mounting a semiconductor die ~~facedown~~ face down to an interposer substrate in a flip ~~chip~~ chip-type semiconductor device assembly according to the present invention;

Please amend paragraph **[0035]** as follows:

[0035] FIG. 10 illustrates dispensing filler material through an opening in an interposer substrate in a flip ~~-chip-~~ chip-type semiconductor device assembly according to the present invention to fill recesses therein;

Please amend paragraph **[0036]** as follows:

[0036] FIG. 11 illustrates encapsulating a semiconductor die in a flip ~~-chip-~~ chip-type semiconductor device assembly and attaching the flip ~~-chip-~~ chip-type semiconductor device assembly according to the present invention to another substrate via solder balls;

Please amend paragraph **[0037]** as follows:

[0037] FIG. 12 illustrates a cross-sectional side view of a flip ~~-chip-~~ chip-type semiconductor device assembly including a heat transfer element according to the present invention;

Please amend paragraph **[0038]** as follows:

[0038] FIGS. ~~13A—13B-~~ 13A and 13B illustrate a method of assembling the flip ~~-chip~~ chip-type semiconductor device assembly according to the present invention at a wafer level, wherein: FIG. 13A illustrates a wafer positioned ~~-facedown-~~ face down prior to being attached to a wafer scale interposer substrate of the present invention; and FIG. 13B illustrates the wafer attached ~~-facedown-~~ face down to the wafer scale interposer substrate;

Please amend paragraph **[0041]** as follows:

[0041] FIG. 16 illustrates underfilling and encapsulating a flip chip-type semiconductor device assembly wherein the bumps on the semiconductor die and the recesses formed in the interposer substrate are arranged in a peripheral configuration according to the present invention;

Please amend paragraph **[0046]** as follows:

[0046] The interposer substrate 110 may be formed from any known substrate material and is preferably formed of, by way of example, a flexible laminated polymer or polyimide layer, such as UPILEX®, produced by Ube Industries, Ltd., or any other polymer-type layer. The interposer substrate 110 may also be made of a bismaleimide triazine (BT) resin, ~~FR-4, FR-5~~ FR4, FR5 or any type of substantially nonflexible material, such as a ceramic or epoxy resin.

Please amend paragraph **[0048]** as follows:

[0048] The multiple recesses 120 are formed in the interposer substrate 110 in a preselected pattern to correspond with a bond pad configuration formed on an active surface of a semiconductor die intended to be attached thereto. For example, FIG. 1 depicts the multiple recesses 120 in a centrally aligned, single-row configuration in interposer substrate 110. Such configuration is made to correspond and attach to a bumped semiconductor die having a centrally aligned, single-row bond pad configuration which will be more fully illustrated hereafter. Other preselected patterns, by way of example, may include an I-shaped recess configuration (FIG. 14) or a peripheral recess configuration (FIG. 15); however, the present invention may be adapted to any recess configuration to match with any particular, desired bond pad configuration. In addition, the multiple recesses 120 may be formed in any suitable shape, such as square, rectangular and circular, and may include tapered sidewalls so that the openings or ~~mouths~~ mouths 120m of the recesses 120 are larger than the bottoms thereof.

Please amend paragraph **[0049]** as follows:

[0049] It will be observed in FIG. 1 that conductive traces 124 extend over recesses 120 and may optionally extend therebeyond, if desired, for enhanced adhesion of conductive traces 124 to dielectric substrate member 111. Conductive pads or terminals 122 may completely cover the bottoms of recesses 120 or, as depicted in FIG. 1, may be narrower than recesses 120 at the bottoms thereof so that gaps 121 are defined on one or both sides of conductive pads or terminals 122. As implied above, the conductive traces 124, which may, for example, comprise copper or a copper alloy, may be adhered to the dielectric substrate member of UPILEX®, BT

resin, ~~FR-4 or FR-5~~ FR4 or, FR5 laminate material, or other substrate materials, using adhesives as known in the art. In some instances, the material of the conductive ~~traces~~ traces 124 may be adhesively laminated to the dielectric substrate member in the form of a conductive sheet, the traces then being subtractively formed from the conductive sheet, as by etching.

Please amend paragraph **[0054]** as follows:

[0054] FIG. 4B depicts dielectric substrate member 111 with one of the recesses 120 formed therein. Such recesses 120 may be formed by patterning, utilizing a chemical wet etch or dry etch, mechanical drilling or punching, laser ablation, or any method known in the art and suitable for use with the type of material employed for the dielectric substrate member 111. The recesses 120 are preferably formed to expose portions of one of the conductive traces 124, such as conductive pads or terminals 122. At a bottom of each recess 120 and, for example, at the location of each conductive pad or terminal 122, additional conductive material may be placed, such as gold or eutectic tin/lead solder, the material selected being compatible with the conductive material of the conductive traces 124 and with the bumps of a semiconductor die to be mated with interposer substrate 110. FIG. 4C illustrates that the walls of the recesses 120 may include a conductive layer 123 formed thereon, for example, by electroless plating; however, such plating is not required for practice of the present invention. ~~Further~~ Further, and as shown in FIGS. 4B and 4C, recesses may be formed with large mouths which taper to a smaller bottom. Such tapering may be easily effected using isotropic etching techniques as known in the art.

Please amend paragraph **[0056]** as follows:

[0056] FIGS. ~~6A – 6B~~ 6A and 6B depict simplified cross-sectional views of a first method of mounting and bonding interposer substrate 110 to a semiconductor die 150 in a flip chip-type semiconductor device assembly 160. FIG. 6A illustrates the first surface 112 of interposer substrate 110 aligned and facing the semiconductor die 150 prior to the assembly thereof. Semiconductor die 150 includes an active surface 152 and a back side or surface 154, wherein the active surface 152 includes a plurality of bond pads 158 bearing electrically conductive bumps 156 thereon. Such conductive bumps 156 and bond pads 158 of

semiconductor die 150 are of a preselected configuration, wherein the recesses 120 in interposer substrate 110 are sized and configured to correspond with the configuration of the bond pads 158 and conductive bumps 156 of semiconductor die 150 so that the respective configurations or patterns of recesses 120 and conductive bumps 156 are substantially mirror images of each other. As shown, solder mask 118 may have an opening 130 defined therethrough or, alternatively, full solder ~~mask~~ mask 118 coverage may be provided across the bottoms of conductive traces 124, including the locations of recesses 120 as previously described with respect to FIGS. 5A through 5D.

Please amend paragraph **[0058]** as follows:

[0058] FIGS. ~~6A - 6B~~ 6A and 6B depict simplified cross-sectional views of a first method of mounting and bonding interposer substrate 110 to a semiconductor die 150 in a flip chip-type semiconductor device assembly 160. FIG. 6A illustrates the first surface 112 of interposer substrate 110 aligned and facing the semiconductor die 150 prior to the assembly thereof. Semiconductor die 150 includes an active surface 152 and a back side or surface 154, wherein the active surface 152 includes a plurality of bond pads 158 bearing electrically conductive bumps 156 thereon. Such conductive bumps 156 and bond pads 158 of semiconductor die 150 are of a preselected configuration, wherein the recesses 120 in interposer substrate 110 are sized and configured to correspond with the configuration of the bond pads 158 and conductive bumps 156 of semiconductor die 150 so that the respective configurations or patterns of recesses 120 and conductive bumps 156 are substantially mirror images of each other. As shown, solder mask 118 may have an opening 130 defined therethrough or, alternatively, full solder ~~mask~~ mask 118 coverage may be provided across the bottoms of conductive traces 124, including the locations of recesses 120 as previously described with respect to FIGS. 5A through 5D.

Please amend paragraph **[0059]** as follows:

[0059] FIGS. ~~7A - 7B~~ 7A and 7B depict simplified cross-sectional views of a second method of mounting and bonding interposer substrate 110 to a semiconductor die 150 in a flip

chip-type semiconductor device assembly 160. FIG. 7A illustrates the first surface 112 of interposer substrate 110 aligned with and facing the semiconductor die 150 prior to the assembly thereof. FIG. 7A is similar to FIG. 6A in substantially every respect, except the conductive bumps 156 on the semiconductor die 150 carry a conductive paste 182 thereon. Such conductive paste 182 may be provided on the bumps by dipping the conductive bumps 156 into a pool of conductive paste 182 or by depositing, dispensing or otherwise transferring the conductive paste 182 to the conductive bumps 156. The conductive paste 182 may include, but is not limited to, eutectic solder, conductive epoxy, or any nonsolid conductive material known in the art. As shown, solder mask 118 may have an opening 130 defined therethrough or, alternatively, full solder ~~mask~~ mask 118 coverage may be provided across the bottoms of conductive traces 124, including the locations of recesses 120 as previously described with respect to FIGS. 5A through 5D.

Please amend paragraph **[0060]** as follows:

[0060] As depicted in FIG. 7B, the interposer substrate 110 is mounted to semiconductor die 150 to form flip chip-type semiconductor device assembly 160, wherein each of the conductive bumps 156 is substantially inserted into a corresponding recess 120 of interposer substrate 110 with the conductive paste 182 engaging with the conductive pad or terminal 122 in each of the recesses 120. With this arrangement, the conductive paste 182 provides contact with the conductive pads or terminals 122 even if some of the conductive bumps 156 are inconsistent in height, *i.e.*, their free ends are noncoplanar. Such conductive bumps 156 having the conductive paste 182 provided thereon may then be bonded to the conductive pads or terminals 122 in the recesses 120 of interposer substrate 110 as previously described in association with FIGS. 6A and 6B.

Please amend paragraph **[0062]** as follows:

[0062] With the conductive paste 182 in the recesses 120, FIG. 8C depicts the interposer substrate 110 mounted to semiconductor die 150 to form flip chip-type semiconductor device assembly 160, wherein each of the conductive bumps 156 is substantially inserted into the

conductive paste 182 in the corresponding recess 120 of interposer substrate 110. As previously described in FIG. 7B, the conductive paste 182 provides electrical and mechanical interconnection between the conductive pads or terminals 122 or trace ends and the conductive bumps 156 even if some of the conductive bumps 156 are inconsistent in height, *i.e.*, their free ends are noncoplanar. The semiconductor die 150 may then be bonded with the interposer substrate 110 as previously described in association with FIGS. 6A and 6B. It will be understood, as noted above, that stencil 186 may not be required if the mass of conductive paste 182 is disposed and spread into recesses 120 prior to disposition of an adhesive element 116 over first surface 112. Moreover, it will be understood that conductive paste 182, if eutectic solder, may be disposed in recesses 120 and then reflowed and solidified prior to attachment of semiconductor die 150 to interposer substrate 110 using a second reflow to provide an indefinite shelf life for interposer substrate 110. Alternatively, semiconductor die 150 may be aligned with interposer substrate 110 after conductive paste disposition and a single reflow may be employed. FIG. 8D is an enlarged view of a single conductive bump 156 carried by a semiconductor die 150 in initial contact with a mass of conductive paste 182 disposed in a recess 120 in dielectric substrate member 111 of interposer substrate 110 over conductive pad or terminal 122 of a conductive trace 124.

Please amend paragraph **[0063]** as follows:

[0063] As a further alternative, a conductive bump 156 to be used either in cooperation ~~with or in lieu of~~ with, or in lieu of, a conductive bump 156 carried by semiconductor die 150 may be formed in each of recesses 120 through plating of conductive pads or terminals 122 with a conductive material such as a suitable metal. Such plating may be effected electrolytically, using a bus line connected to each conductive trace 124, or by electroless plating, both techniques being well known in the art.

Please amend paragraph **[0064]** as follows:

[0064] FIGS. ~~9A–9B~~ 9A and 9B depict simplified cross-sectional views of a variant of the above-described third method comprising a fourth method of preparing, mounting and

bonding interposer substrate 110 to a semiconductor die 150 in a flip chip-type semiconductor device assembly 160. Such variant is similar to the third method as described in FIGS. 8A - 8D of providing conductive paste 182 in each of the recesses 120, except the conductive bumps 156 are initially unattached to the bond pads 158 of the semiconductor die 150. As depicted in FIG. 9A, the conductive bumps 156 in the form of balls, such as metal balls, are embedded into the conductive paste 182, which was previously spread into the recesses 120 of the interposer substrate 110. The bond pads 158 in the semiconductor die 150 are aligned with the conductive bumps 156 in the recesses 120 in the interposer substrate 110 and then mounted thereto, as depicted in FIGS. ~~9A– 9B,~~ 9A and 9B. The conductive paste 182 may comprise a solder wettable to both bond pads 158 and conductive pads or terminals 122 or a conductive or conductor-filled adhesive. It will also be understood and appreciated that conductive bumps 156 may themselves comprise solder, such as a PbSn solder, and conductive paste 182 may be, optionally, eliminated.

Please amend paragraph **[0066]** as follows:

[0066] It will be well appreciated by one of ordinary skill in the art that, since the conductive bumps 156 are bonded within the recesses 120 of the interposer substrate 110 itself, the height of the flip chip-type semiconductor device assembly 160 is minimized. Therefore, conductive bumps 156 may be formed larger in size than those of conventional flip chip assemblies without increasing, or even while decreasing, the height of the flip chip-type semiconductor device assembly 160, resulting in the increase in electrical and mechanical reliability and performance of the interconnections between the interposer substrate 110 and the semiconductor die 150. Further, the recesses 120 in the interposer substrate 110 provide an inherent alignment aspect absent in a conventional flip ~~chip~~ chip-type semiconductor device assembly because the conductive bumps 156 easily slide into their respective corresponding recesses 120 to ensure proper alignment and proper attachment thereof. In addition, the adhesive element 116 on the first surface 112 of the interposer substrate ~~110~~ 110, as well as the conductive paste 182 in the recesses ~~120~~ 120, may act as a height controller for reliable attachment of the semiconductor die 150 to the interposer substrate 110, wherein the adhesive

element 116 and/or the conductive paste 182 may be used to compensate for any irregularities due to varied conductive bump sizes, recess depths and planarity variation in the surfaces of the interposer substrate 110 and semiconductor die 150.

Please amend paragraph **[0067]** as follows:

[0067] As shown in FIG. 10, a dielectric filler material 166 (commonly termed an "underfill" material) may be optionally applied through opening 130. The method employed to apply the dielectric filler material 166 is preferably by dispensing under pressure from dispenser head 164, but may include any method known in the art, such as gravity and vacuum injecting. In this manner, the dielectric filler material 166 may be applied into the opening 130, move as a flow front through the multiple segments 132 (see FIG. 2) and into each of the recesses 120 to fill a space around the conductive bumps 156, bond pads 158 and conductive pads or terminals 122. The dielectric filler material 166 may be self-curing through a chemical reaction, or a cure accelerated by heat, ultraviolet light or other radiation, or other suitable means may be used in order to form at least a semisolid mass in the recesses 120. Such dielectric filler material 166 provides enhanced securement of the components of flip chip-type semiconductor device assembly 160 as well as precluding shorting between conductive elements and protecting the conductive elements from environmental concerns, such as moisture. As such, compared to the conventional underfilling of the entire semiconductor die, the flip chip-type semiconductor device assembly 160 of the present invention requires less time since the filler material may only be directed to fill the recesses 120 or, rather, any leftover space within the recesses 120 proximate the interconnections, *i.e.*, conductive bumps 156.

Please amend paragraph **[0071]** as follows:

[0071] FIG. 12 depicts a flip chip-type semiconductor device assembly 160 including a heat transfer element 180. The heat transfer element 180 may be provided over the first surface 112 of the interposer substrate 110 and under the adhesive element 116 as a thin, thermally conductive material. The heat transfer element 180 may also be provided on the active surface 152 of the semiconductor die 150 to abut the first surface 112 of the interposer

substrate 110. Another option is to provide the heat transfer element 180 on the back side or surface 154 of the semiconductor die 150 as shown in broken lines. Such heat transfer element 180 is configured and located to thermally conduct heat generated from the electrical components of the semiconductor die 150 to remove such heat from the flip chip-type semiconductor device assembly 160 and to reduce the incidence of thermal fatigue in the interconnections and circuitry of the flip chip-type semiconductor device assembly 160 and, specifically, the semiconductor die ~~150~~ 150, as well as to reduce operating temperatures. The heat transfer element 180 may be formed of any thermally conductive material, such as copper and silver, but may also comprise a thermally conductive material that is nonelectrically conductive, such as a thin diamond material and/or diamond composite deposited as a thin film or layer.

Please amend paragraph **[0073]** as follows:

[0073] The interposer substrate 210 includes a first surface 212 and a second surface 214 with multiple recesses 220 formed in the first surface 212 and openings 230 having passages (not shown) formed in the second surface 214. The recesses 220 formed in the interposer substrate 210 are made to correspond in substantially a mirror image with the bump configuration on each of the multiple semiconductor dice 251 of the semiconductor wafer 250. In this manner, the interposer substrate 210 may be attached to the semiconductor wafer 250 via an adhesive element 216 on the first surface 212 of the interposer substrate 210 so that the conductive bumps 256 on the semiconductor wafer 250 are inserted into and substantially received within the multiple recesses 220 formed in the interposer substrate 210 to form a wafer scale assembly 260, as depicted in FIG. 13B. The wafer scale assembly 260 may then be singulated or "diced" along the borders 253 of the semiconductor wafer 250 via a dicing member such as a wafer saw 280 to form individual, singulated flip ~~chip~~ chip-type semiconductor device assemblies that each include one or more semiconductor dice 251 having the separated interposer substrate 210 of the present invention mounted thereon.

Please amend paragraph **[0074]** as follows:

[0074] Also at the wafer level and as previously described in association with FIGS. ~~6A-6B, 7A-7B, 8A-8D,~~ 6A, 6B, 7A, 7B, 8A - 8D, and ~~9A-9B,~~ 9A, 9B, the conductive bumps 256 may be bonded to the conductive pads or terminals in the recesses 220 to, therefore, mechanically bond and electrically connect the semiconductor wafer 250 to the wafer scale interposer substrate 210. In addition, dielectric filler material may be applied through the openings 230 and conductive balls 262 may be provided on the bond posts on the second surface 214 of the interposer substrate 210, either prior to dicing the wafer scale assembly 260 or subsequent thereto.

Please amend paragraph **[0075]** as follows:

[0075] FIG. 14 depicts a top plan view of an interposer substrate 310 having an alternative recess configuration made for corresponding to a substantially "mirror image" bond pad configuration on the active surface of a semiconductor die. In particular, in this first alternative, there is an I-shaped bond pad configuration, wherein multiple recesses 320 are formed over the upper surface 312 of interposer substrate 310 that are aligned in the shape of an "I" with adhesive elements 316 disposed on either side of the body of the "I" and between the ends thereof. In another alternative recess configuration, the ~~recesses~~ recesses 320 may be formed in an interposer substrate around a periphery thereof. Such alternative is depicted in FIG. 15 of a top plan view of an interposer substrate 410 with an adhesive element 416 at a center portion of interposer substrate 410 and recesses 420 formed thereabout and proximate a periphery of interposer substrate 410. As in the previous recess configurations, the periphery recess configuration in interposer substrate 410 is made to correspond with a substantially "mirror image" bond pad configuration on an active surface of a semiconductor die.

Please amend paragraph **[0077]** as follows:

[0077] FIG. 16 depicts a cross-sectional view of a flip chip-type semiconductor device assembly 460 including a semiconductor die 450 mounted ~~facedown~~ face down to an interposer substrate 410 having a peripheral recess configuration and an alternative method of applying

dielectric filler material 166 to the flip chip-type semiconductor device assembly 460. In particular, dielectric filler material 166 may be applied by dispenser head 164 around the periphery of the semiconductor die 450 so that the dielectric filler material 166 flows under the semiconductor die 450 and around the conductive bumps 456 adjacent the semiconductor die 450 periphery. As such, the dielectric filler material 166 is only needed proximate the conductive bumps 456 and not under the entire die as done conventionally. The semiconductor die 450 may be left exposed or encapsulated by encapsulation apparatus 178, which may provide encapsulation material 168 to the flip chip-type semiconductor device assembly 460 via dispensing, spin-coating, glob-topping, depositing or transfer molding, or any suitable method known in the art. It is preferred that such encapsulation material 168 be applied to the back surface 454 of the semiconductor die 450 at the wafer level or prior to dispensing the dielectric filler material 166 about the periphery to facilitate fully encapsulating the semiconductor die 450.

Please amend paragraph **[0078]** as follows:

[0078] Further, in this alternative embodiment, it is preferred that the semiconductor die 450 is assembled and bonded to the interposer substrate 410 with the conductive bumps 456 disposed in the conductive paste 182 as described in FIGS. 8A - 8D and ~~9A - 9B;~~ 9A, 9B; however, this alternative may also employ the methods described in FIGS. ~~6A - 6B and 7A - 7B~~ 6A, 6B, and 7A, 7B for assembling and bonding the semiconductor die 450 to the interposer substrate 410.

Please amend paragraph **[0082]** as follows:

[0082] Thus, it will be apparent that the flip ~~chip~~ chip-type semiconductor device assembly of the present invention provides a compact, robust package at a reduced cost in comparison to conventional bumped semiconductor die assemblies employing dual conductive layer interposers. For example, a package height reduction of about 90 μm may be effected using a 100 μm thick dielectric member and eliminating a second 12 μm thick conductive layer adjacent the semiconductor die, even with a 25 μm thick adhesive element comprising a tape disposed between the semiconductor die and the interposer substrate, since the discrete

conductive elements or conductive bumps of the die may be substantially completely received within the recesses of the dielectric member, but for any vertical standoff provided by the tape. Electrical connection reliability is improved, since the conductive bumps are in contact with the terminals at the recess bottoms, either directly or through an interposed conductive material within the recesses, eliminating the need for conductive vias and an electrical connection between a first conductive layer adjacent the semiconductor die contacted by a conductive bump and a via and another electrical connection between the via and a second conductive layer on the opposite side of the interposer substrate. Moreover, due to the straightforward design, even large semiconductor dice carrying a large number of conductive bumps may be rerouted for external connection using the present ~~invention~~ invention, as all rerouting is carried out on the side of the interposer substrate facing away from the semiconductor die.

Please amend paragraph **[0085]** as follows:

[0085] In addition, the use of a flexible interposer substrate easily accommodates minor variations between heights of various conductive bumps and lack of absolute planarity of the semiconductor die active ~~surface~~ surface, as well as that of the terminals. Further, encapsulation, if desired, of some or all portions of the periphery and back surface of the semiconductor die by a variety of methods is greatly facilitated, as is incorporation of a thermally conductive heat transfer element such as a heat ~~sink~~ sink, without adding complexity to the package. If an adhesive element employing a tape is used to secure the semiconductor die and interposer substrate together, different bond pad arrangements are easily accommodated without the use of a liquid or gel adhesive and attendant complexity of disposition. More specifically, during semiconductor die placement, the tape may act as a stopper or barrier and as a cushion. If a conductive paste is deposited in a via, the tape acts as a barrier to prevent paste contamination of the surface of the semiconductor die. If, on the other hand, solidified conductive bumps are ~~used,~~ used when heat is used to soften the bump material, the tape acts as ~~a stopper~~ stopper, as well as ~~a cushion~~ cushion, when the bump material relaxes. In addition, tape accommodates the "spring back" effect exhibited when force used to assemble a semiconductor die and interposer

substrate is released, helping to keep the interconnection or joint together. These advantages are applicable to both rigid or flexible interposer substrates.